ARIA Sensing® by Cover Sistemi

LT103OEM_XG Radar Module

Rev.1.1

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Author: Technical Office

POC: info@ariasensing.com

Version for public release; specifications are subject to change without notice to improve reliability, function, or design or otherwise.

LT103OEM_XG Radar Module

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1 Summary

- The LT103OEM is a complete micro-UWB radar module designed for SMD mounting.
- The LT103OEM_XG is a convenient PCB with an LT103OEM already mounted and providing pin headers for the connection of the LT103OEM to a PC, for quick assessment of the LT103OEM performances or a rapid development of custom algorithms and applications.

Table of contents

2 Reference Documents

1. LT103OEM Datasheet
2. LT102 and LT103OEM COM Protocol

3 Document Scope

This document is relevant to the designers involved in the development of radar algorithms over the LT103OEM module or in the evaluation of LT103OEM performances.

4 Description

The LT103OEM_XG is basically a board holding an LT103OEM and connecting the LT103OEM signals to a standard 2.54mm-pitch pin header.

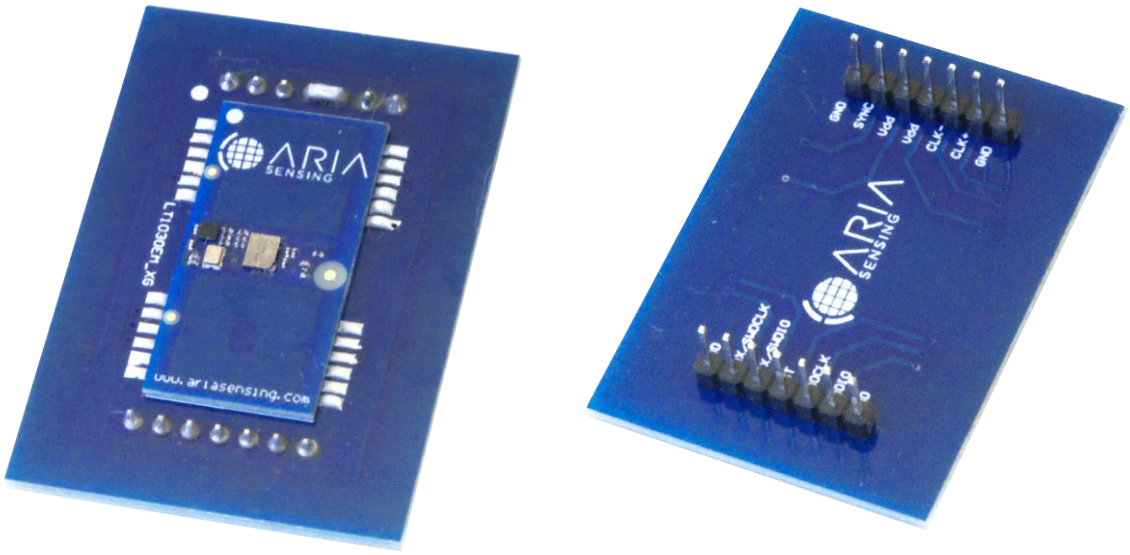

Fig. 1: LT103OEM_XG; Top view (left) and Bottom view (right)

5 Electrical specifications

	Min	Typ	Max
Operating frequency	7.3GHz	7.9GHz	8.5GHz
Temperature range	-40°C		+85°C
Supply voltage (Vdd_{RF})	1.8V	3.3V	3.6V
Supply voltage (Vdd_{DIG})	1.8V	3.3V	3.6V

Supply current (Idd_{RF}+Idd_{DIG})			85 mA
Range resolution		7 mm	
V_{IL}	0		0.3 · Vdd_{DIG}
V_{IH}	0.7 · Vdd_{DIG}		Vdd_{DIG}
V_{OL} (I_{OL}=0 mA)	0.0		
V_{OH} (I_{OH}=0 mA)			Vdd_{DIG}
R_{series} IO (protection resistors, UART, SWDIO and SWDCLK)		220 Ohm	

Table 1 LT103OEM_XG electrical specifications

6 Pin-out

PIN number	Description
1 GND	Ground (all ground pins are shorted internally)
2 Clk+	Radar front-end LVDS Clock, positive pin (specialized function, leave open)
3 Clk-	Radar front-end LVDS Clock, negative pin (specialized function, leave open)
4 Vdd	1.8V-3.3Vdc VddANA (internally shorted to VddDIG)
5 Vdd	1.8V-3.3Vdc VddDIG (internally shorted to VddANA)
6 SYNC	Multi radar Sync pin (specialized function, leave open)
7 GND	Ground (all ground pins are shorted internally)
8 GND	Ground (all ground pins are shorted internally)
9 URX/SWDCLK	UART Rx (SWDCLK when LT103OEM blank)
10 UTX/SWDIO	UART Tx (SWDIO when LT103OEM blank)
11 RST	Reset (active low)
12 SWDCLK	SWDCLK (with FW loaded). Not needed (leave open)
13 SWDIO	SWDIO (with FW loaded). Not needed (leave open)
14 GND	Ground (all ground pins are shorted internally)

Table 2 LT103OEM_XG Pin-out

7 PC Connection

It is possibile to use an FTDI P/N C232HM-DDHSL-0 to connect the LT103OEM_XG.
A convenient set of Octave/Matlab scripts can be provided for the low-level communication between PC and LT103OEM_XG. Alternatively, a Windows 10 User Interface program is provided. Connection scheme is reported in Table 3.

C232HM cable	LT103OEM+XG Pin
--------- (red)	Vdd any (Vdds shorted)
--------- (black)	GND (any)
--------- (orange)	URX/SWDCLK
--------- (yellow)	UTX/SWDIO
--------- (green)	RST*

Table 3 Connection scheme

(*) RST may be left unconnected. It is required only when updating FW.

8 Internal connection scheme

The internal connection scheme is reported in the next picture.

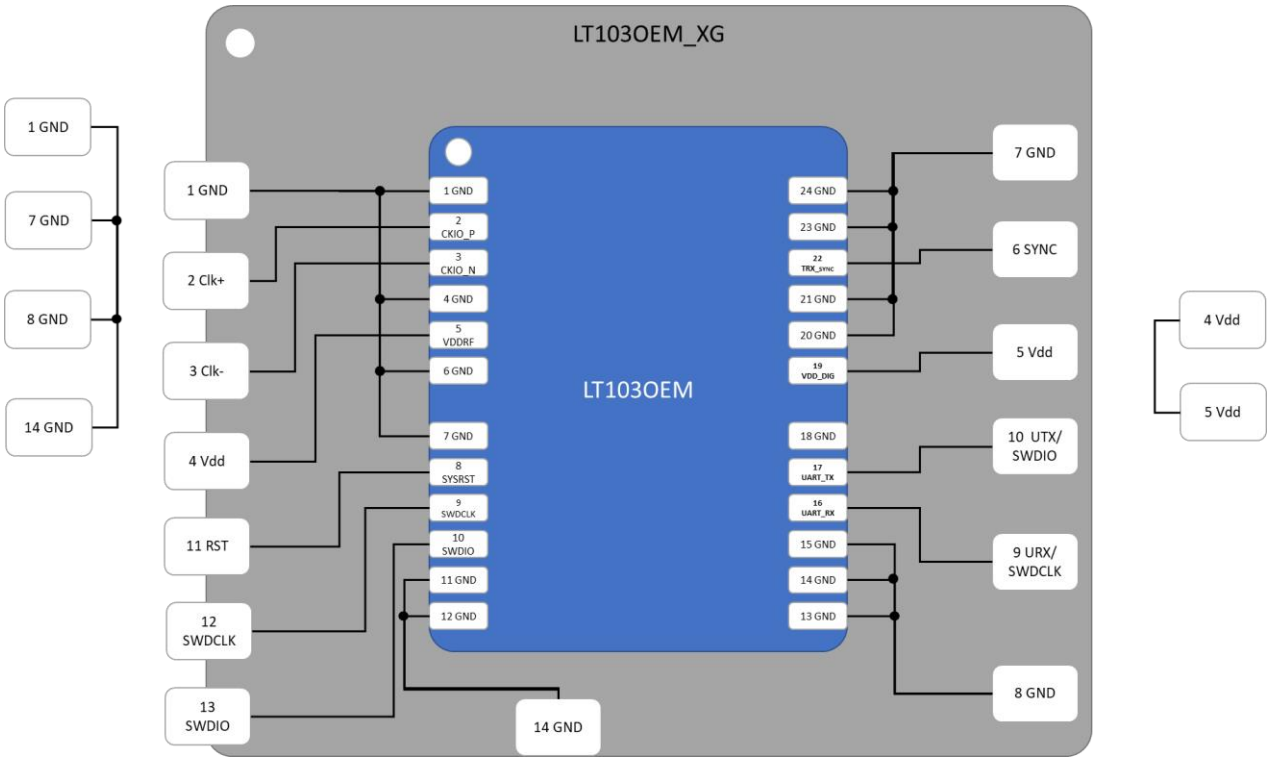

Fig. 2: internal connection scheme for LT103OEM_XG

8.1 Layout

The layout of the LT103OEM_XG is identical to the suggested layout for any board adopting the LT103OEM.

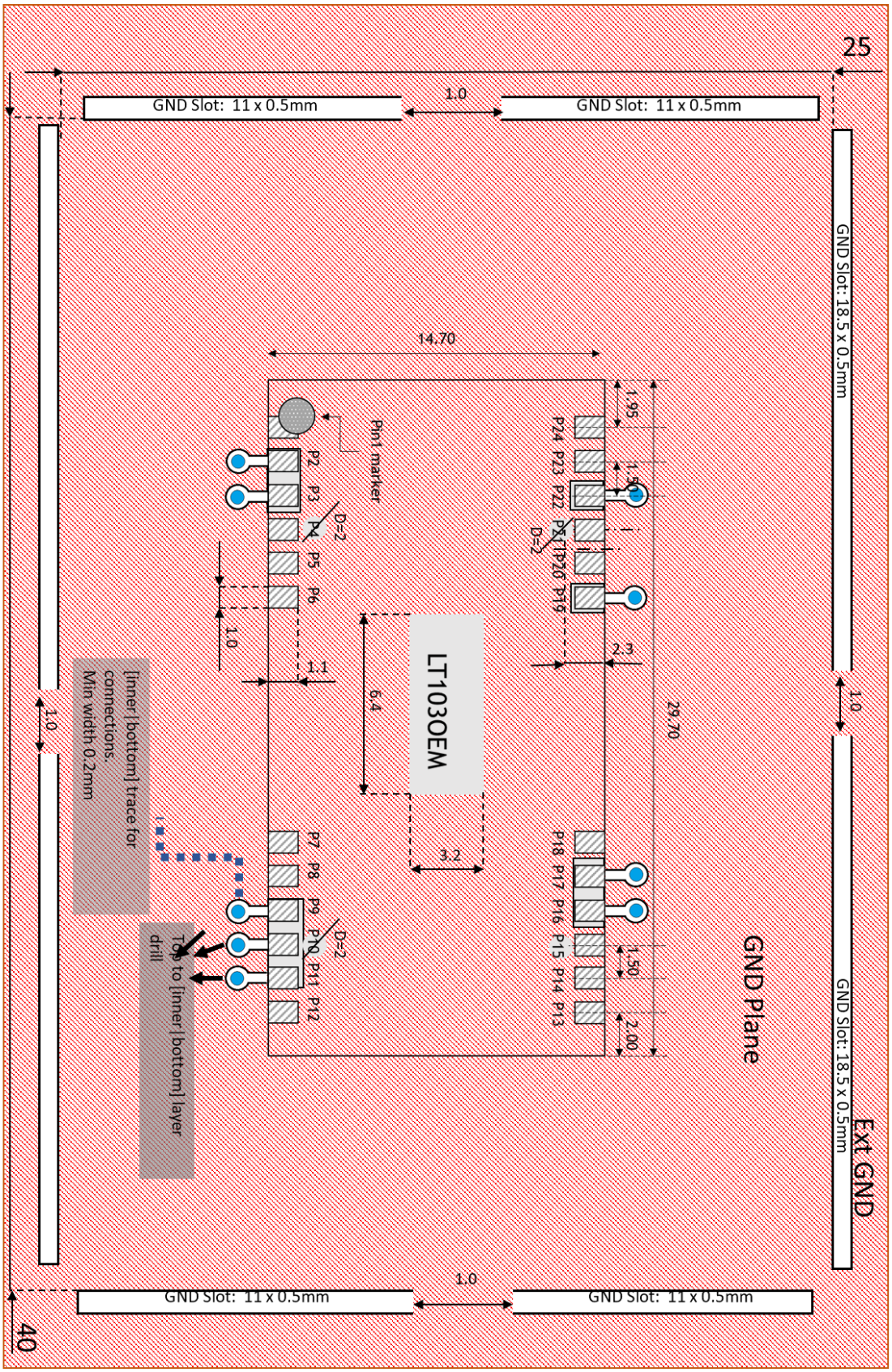

Fig. 3 Suggested Layout for any board adopting LT103OEM